[Total No. of Questions - 9] [Total No. of Printed Pages - 2]

Dec.-22-0319

EC-704 (VLSI Design)

B.Tech. 7th (CBCS)

Time : 3 Hours **Max. Marks : 60**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt Five questions in all, selecting one question from each Section A, B, C and D. Section E is compulsory. Answer should be brief and to the point and be supplemented with the neat sketches.

SECTION - A

1. Explain the construction and working of enhancement and depletion type MOSFETs with neat and clean diagrams. (10)

2. Explain the following terms for a MOS device:- (10)

   (a) Graphically represent the region of operation of MOSFET.

   (b) Define the condition of weak and strong inversion in relation to surface potential.

   (c) Impact of effective mobility on device performance

   (d) Differentiate between n and p channel MOSFET.

SECTION - B

3. Calculate the static power dissipation for CMOS inverter and pseudo-nMOS inverter with pMOS as a load. And compare the static power dissipation for both the inverters (make proper diagrams wherever required). (10)

4. Compare the performance of 2 input NAND and NOR gate for unit inverter size just by keepings $\mu_n=2\mu_p$. And implement the same using dynamic technique. (10)

SECTION - C

5. What are physical design rules in IC design process? And also provide the importance of physical design rules in IC fabrication. (10)

6. Explain the working of 6T SRAM cell and mark the components offering leakage current in schematic diagram. (10)

SECTION - D

7. For Fig 1. Using small signal model analysis calculate the output resistance and gain. (10)

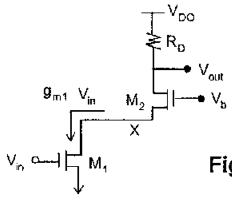

Fig. 1

8. Calculate the voltage gain and output resistance for the differential amplifier designed using MOS technology. (10)

SECTION - E

9. Short answer type (limit 20-40 words only).

   (a) Explain the operation of C.S. amplifier, when the load is:- (a) resistive load (b) Diode load (c) current source load.

   (b) In which technology, Intel i3 and i5, processors are fabricated?

   (c) What is LVS?

   (d) What is the importance of transconductance in amplifier design?

   (e) Define the threshold voltage for p-channel MOSFET.

   (f) What are the advantages of CMOS process?

   (g) What is advantage of CMOS over BJT technology?

   (h) How many types of parasitic components are possible in CMOS device?

   (i) What size of contact & vias are allowed on a chip?

   (j) Which is the significance of term lambda? (10×2=20)